CIRCUITS AND METHODS FOR DATA MULTIPLEXING

ABSTRACT

A method and apparatus for data multiplexing is capable of high-speed operation with acceptable timing margins and has reduced sensitivity to supply voltage, temperature, manufacturing and other variations. One implementation relates to a data multiplexer that has no significant speed limitation associated with the clock-to-data delay of data latches, flip-flops, etc. In one implementation, clock-to-data delay is compensated for by introducing a delay-compensator in the clock line that drives a selector stage of the multiplexer. In one such implementation, a timing relationship is established between clock and data waveforms by timing the data waveforms with a first in-phase clock and operating the delay-compensated selector clock line with a second clock, which is delayed with respect to the first clock. The second clock can have a quadrature-phase delay with respect to the in-phase clock.